Hsin-Yu Ting

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EDUCATION

Ph.D. Candidate in Computer Science Sep. 2016 - Present
University of California, Irvine *Irvine, CA*

- Develop the hardware-software co-designed deep learning framework on an embedded FPGA-based heterogeneous SoC architecture, managing diverse computing resources to improve throughput and power efficiency.
- Has developed acceleration system services of programmable hardware in Android operating system, spanning application (Java), Linux kernel (C) and hardware (Verilog) layer.

M.S. in Computer Science Sep. 2011 - August 2013
National Tsing Hua University *HsinChu, Taiwan*

- Designed Elliptic Curve Cryptographic engines for constrained devices, coded in Verilog, and Python for verification. Proposed a scheduling methodology showing efficient resource management on the ECC computation.

WORK EXPERIENCE

Software Engineering Intern: SDx Foundation Libraries June 2019 - Sep. 2019
Xilinx, Inc *San Jose, CA*

- Collaborated in designing Xilinx Vitis accelerated-library for Math, Linear Algebra (i.e. BLAS), providing software APIs to bring plug-n-play acceleration. (https://github.com/Xilinx/Vitis_Libraries)

Software Engineering Intern: I-FPGA Acceleration July 2018 - Sep. 2018
Xilinx, Inc *San Jose, CA*

- Designed algorithm/infrastructure of the software stack on high-performance low-power FPGA accelerators in machine learning. Enabled FPGA acceleration of open source deep learning frameworks, like YOLO.

Software Engineering Intern June 2017 - Sep. 2017
CADWeave *Irvine, CA*

- United cloud-based CAD services on Amazon Web Services (AWS) in product design for mechanical and electronic engineers.

Software Engineer June 2015 - July 2016
Industrial Technology Research Institute *HsinChu, Taiwan*

- Modeled an accelerator-rich architecture into control data flow graphs based on intermediate representation (i.e. LLVM), analyzed/evaluated the computation hotspots with deep learning methods.

Research Assistant Sep. 2014 - June 2016
National Tsing Hua University *HsinChu, Taiwan*

- Investigated the multi-core emulating platform for visual processing and integrated with FPGA boards.

PROJECT

System support for FPGA acceleration service (June 2017 - present)
Develop the software stack that integrates the operating system with programmable hardware and manages the computing resources. Provide the systematic interface between the software application and FPGA designs.

FPGA-based acceleration of climate system model (Oct. 2016 - Sep. 2017)
Deploy the climate system model, Fast J algorithm, in high performance computing to data-rate-aware FPGA-based acceleration using OpenCL, providing improvement across power, performance, programmability.

PUBLICATION

H.-Y. Ting, Tootiya Giyahchi, Ardalan Amiri Sani, Eli Bozorgzadeh, "Dynamic Sharing in Multi-accelerators of Neural Networks on An FPGA Edge Device," in *ASAP*, 2020

H.-Y. Ting, Ardalan Amiri Sani, Eli Bozorgzadeh, "System Services for Reconfigurable Hardware Acceleration in Mobile Devices," in *ReConfig*, 2018

H.-Y. Ting, C.-T. Huang, "Design of Low-Cost Elliptic Curve Cryptographic Engines for Ubiquitous Security," in *VLSI-DAT*, 2014.